S71NS-J

Stacked Multi-Chip Product (MCP)
110 nm CMOS 1.8 Volt-only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory with pSRAM

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71NS-J_00 **Revision** 03 **Issue Date** October 10, 2006

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local Spansion sales office.

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110 nm CMOS 1.8 Volt-only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory with pSRAM

Data Sheet *(Advance Information)*

Features

- **Single 1.8 volt read, program and erase (1.7 to 1.95 V)**
- **Multiplexed Data and Address for reduced I/O count**
  - A15–A0 multiplexed as DQ15–DQ0
  - Addresses are latched by AVD# control input when CE# low
- **Simultaneous Read/Write operation**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
- **Package**
  - 56-ball Very Thin FBGA

Product Selector Guide

MCP	Flash	pSRAM	pSRAM Type	pSRAM Read	OPN
S71NS032JA0	S29NS032J	16 Mb	Mux pSRAM 2	Asynchronous only	S71NS032JA0BJWRT
S71NS032J80	S29NS032J	8 Mb	Mux pSRAM 1	Asynchronous only	S71NS032J80BJWRA

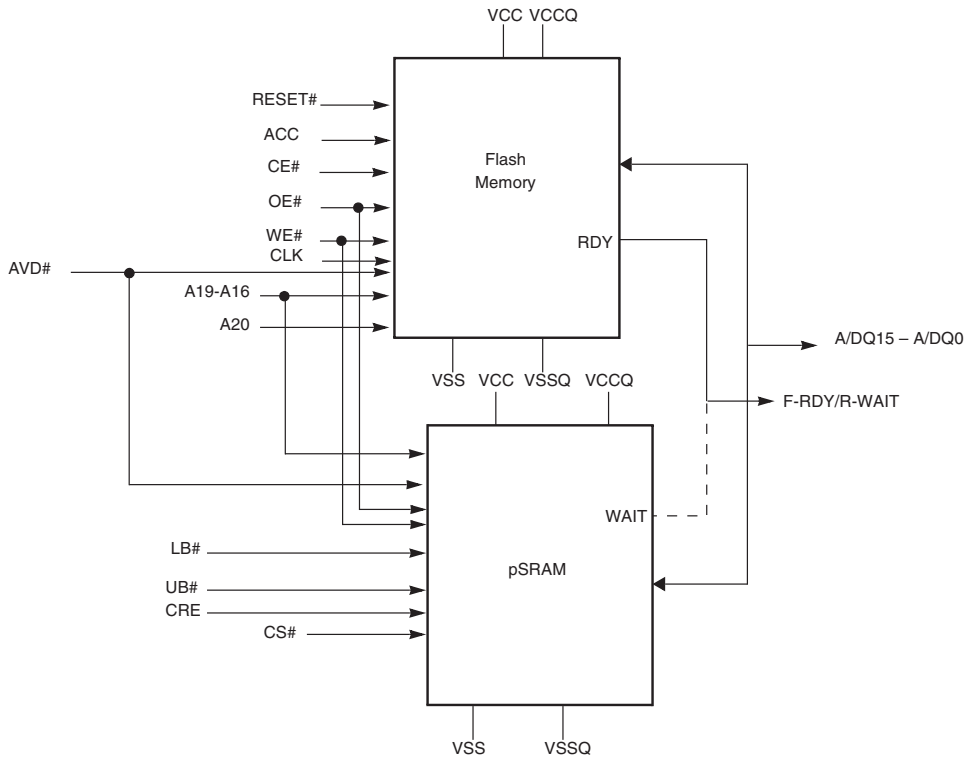
General Description

The products covered by this document are listed in the table below

Document	Publication Identification Number
S29NS-J	S29NS-J_00
8 Mb Multiplexed pSRAM Type 1	muxpsram_06
16Mb Multiplexed pSRAM Type 2 (Asynchronous only)	muxpsram_05

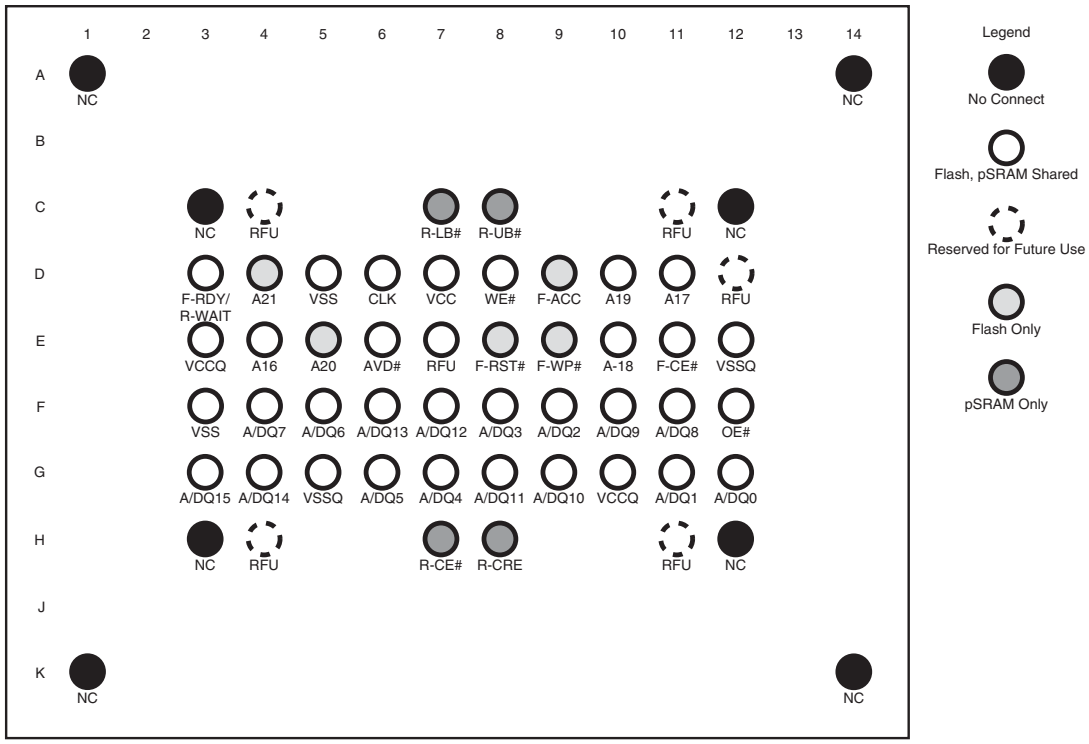
Publication Number S71NS-J_00 **Revision 03** **Issue Date** October 10, 2006

1. MCP Block Diagram



Note:
A19 is shared for S71NS032JA0, but flash only for S71NS032J80.

2. Connection Diagram



MCP	Flash-only Address	Shared Address
S71NS032JA0	A20	A19:A16 ADQ15:ADQ0
S71NS032J80	A20-A19	A18:A16 ADQ15:ADQ0

3. Input/Output Descriptions

Signal	Description	Flash	RAM
R-UB#	pSRAM Upper Byte Control		X
R-LB#	pSRAM Lower Byte Control		X
A21–A16	Address Inputs	X	X
ADQ15–ADQ0	Multiplexed Address/Data input/output	X	X
R-CE#	pSRAM Chip Select Input		X
F-CE#	Flash Chip Enable Input. Asynchronous relative to CLK for the Burst mode.	X	
OE#	Output Enable Input. Asynchronous relative to CLK for the Burst mode.	X	X
WE#	Write Enable Input.	X	X
V_{CC}	Device Power Supply (1.7 V–1.95 V).	X	X
V_{SS}	Ground	X	X
NC	No Connect; not connected internally	X	X
RDY	Ready output; indicates the status of the Burst read. VOL= data invalid. WAIT# pin of pSRAM is shared with Flash RDY pin for synchronous pSRAM.	X	X
CLK	Clock input. The first rising edge of CLK in conjunction with AVD# low latches address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access. CLK is present on MuxpSRAM Type 3, but not on MuxpSRAM Type 2. As a result, it is a shared signal on S71NS064JA0, but a flash-only signal on S71NS032J.	X	X
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs (address bits A15–A0 are multiplexed, address bits A22–A16 are address only). V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs	X	X
F-RST#	Hardware reset input. V_{IL}= device resets and returns to reading array data	X	
F-ACC	At 12 V, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables program and erase functions. Should be at V_{IH} for all other conditions.	X	
R-CRE	Command Register Enable of pSRAM		X
V_{CCQ}	I/O Power Supply (1.7 V to 1.95 V)	X	X
V_{SSQ}	I/O Ground	X	X

4. Ordering Information

The order number (Valid Combination) is formed by the following:

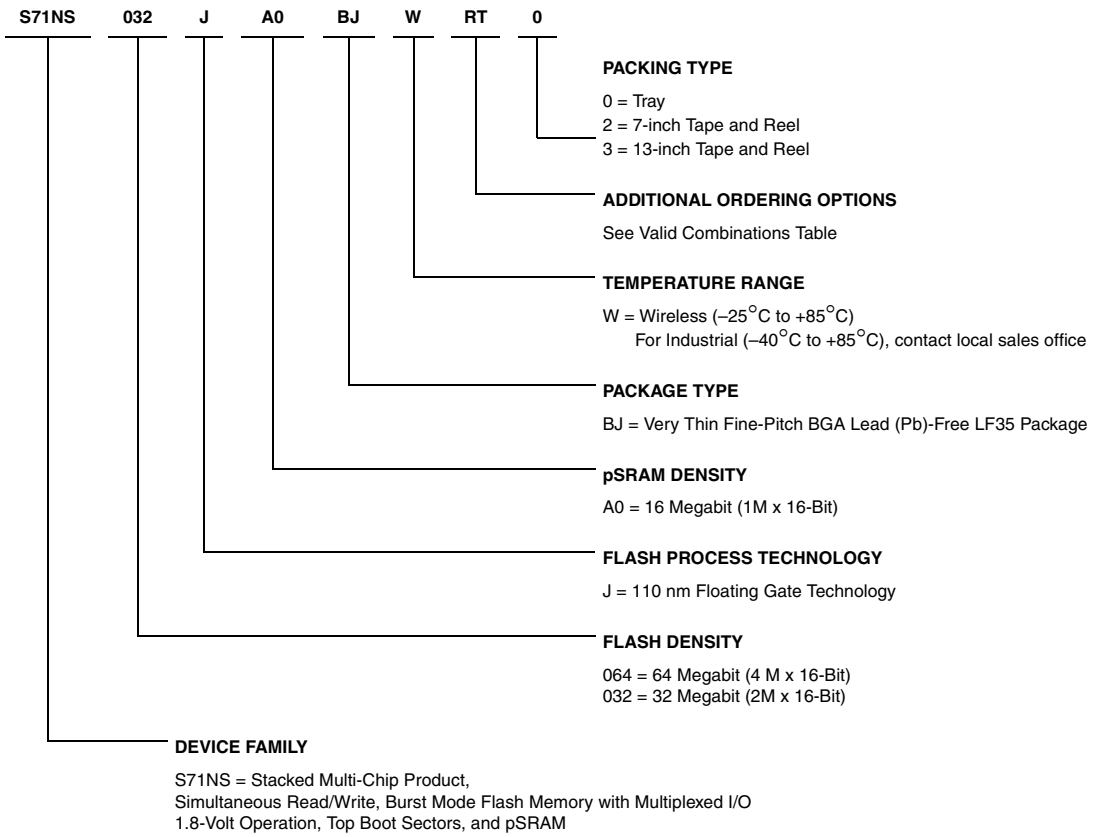
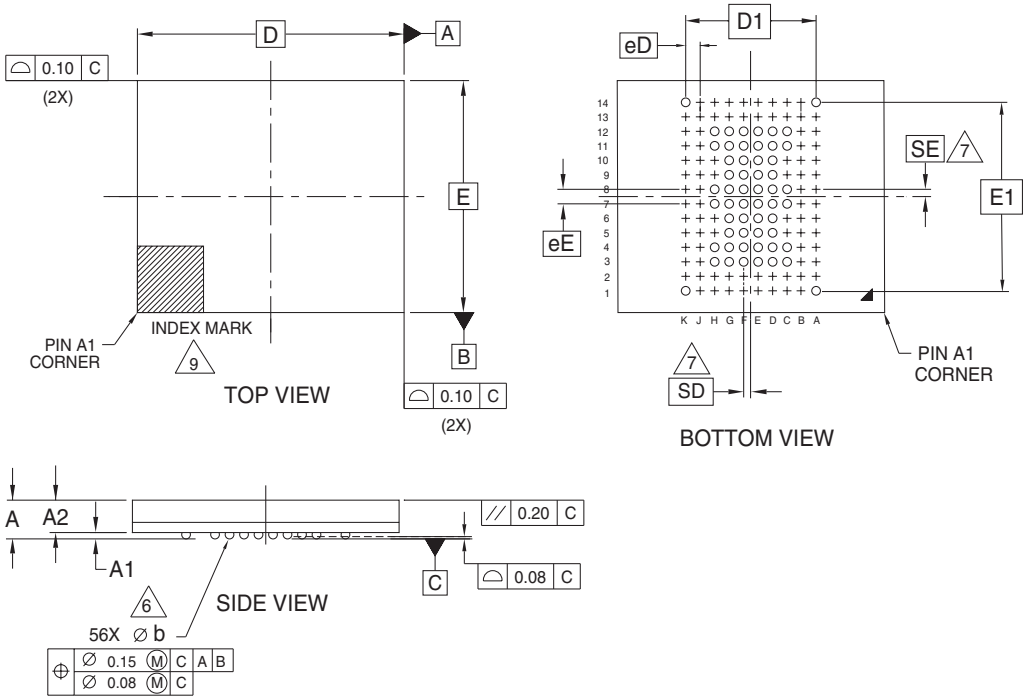


Table 4.1 Valid Combinations

Base OPN	Density	Process Technology	pSRAM Density	Package Type	Temperature	Options	Packing Type
S71NS	032	J	80	BJ	W	RA	0, 2, 3
			A0			RT	

5. Physical Dimensions

5.1 NLB056—56-Ball Very Thin Fine Pitch Ball Grid Array (FBGA) 9.2 x 8.0 mm Package



PACKAGE	NLB 056			
JEDEC	N/A			
D x E	9.20 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.85	---	0.97	BODY THICKNESS
D		9.20 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		4.50 BSC.		MATRIX FOOTPRINT
E1		6.50 BSC.		MATRIX FOOTPRINT
MD		10		MATRIX SIZE D DIRECTION
ME		14		MATRIX SIZE E DIRECTION
n		56		BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE		0.50 BSC.		BALL PITCH
eD		0.50 BSC		BALL PITCH
SD / SE		0.25 BSC.		SOLDER BALL PLACEMENT
	A2 – A13,B1 – B14 C1,C2,C5,C6,C9,C10,C13,C14 D1,D2,D13,D14,E1,E2,E13,E14,F1,F2,F13,F14 G1,G2,G13,G14,H1,H2,H5,H6,H9,H10,H13,H14 J1 – J14, K2 – K13			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

3507\ 16-038.22 \ 7.14.5

6. Revision History

6.1 Revision 01 (March 2, 2006)

Initial release.

6.2 Revision 02 (April 21, 2006)

Added the S71NS032JA0

Updated the MCP Block Diagram

Updated the Connection Diagram notes

Updated the Input/Output Descriptions

6.3 Revision 03 (October 10, 2006)

Added the S71NS032J80

Removed the S71NS064JA0